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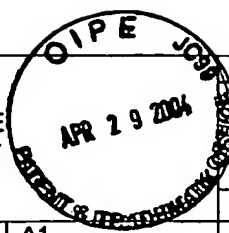
INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet **A1** of **A1**

Complete if Known

Application Number	10/720,042
Filing Date	November 21, 2003
First Named Inventor	Jacob Strom
Group Art Unit	2671
Examiner Name	
Attorney Docket Number	8196-16



U.S. PATENTS AND PATENT PUBLICATIONS					
Examiner Initials*	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY
		Number	Kind Code (if known)		
		US-			
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FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	T
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OTHER NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T
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	2	Cox et al., 1993, Pixel Merging for Object-Parallel Rendering: a Distributed Snooping Algorithm, In <i>Symposium on Parallel Rendering</i> , ACM SIGGRAPH, pp. 49-56	
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	4	Greene et al., 1993, Hierarchical Z-Buffer Visibility, In <i>Proceedings of ACM SIGGRAPH 93</i> , ACM Press/ACM SIGGRAPH, New York, J. Kajiya, Ed., Computer Graphics Proceedings, Annual Conference Series, ACM, pp. 231-238	
	5	Hakura et al., 1997, The Design and Analysis of a Cache Architecture for Texture Mapping, In <i>24th International Symposium of Computer Architecture</i> , ACM/IEEE, pp. 108-120	
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	9	Lathrop et al, 1990, Accurate Rendering by Subpixel Addressing, <i>IEEE Computer Graphics and Applications</i> 10, 5 (September), pp. 45-53	
	10	McCabe et al., 1998, DirectX 6 Texture Map Compression, <i>Game Developer Magazine</i> 5, 8 (August) pp. 42-46	
	11	McCormack et al., 2000, Tiled Polygon Traversal Using Half-Plane Edge Functions, In <i>Workshop on Graphics Hardware</i> , ACM SIGGRAPH/Eurographics, pp. 15-21	
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	14	Nvidia, 2001, HRAA: High Resolution Antialiasing Through Multisampling. Tech rep., pp. 1-8	
	15	Pineda, J., 1988, A Parallel Algorithm for Polygon Rasterization, In <i>Computer Graphics (Proceedings of ACM SIGGRAPH 88)</i> , ACM, pp. 17-20	
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	18	Woo et al., 2002, A 120-mW 3-D Rendering Engine With a 6-Mb Embedded DRAM and 3.2 GB/s Runtime Reconfigurable Bus for PDA Chip, <i>IEEE Journal of Solid-State Circuits</i> 37, 19 (October), pp. 1352-1355.	

Examiner Signature	<i>Sam Brane</i>	Date Considered	11/14/05
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First Named Inventor	Jacob Strom
Group Art Unit	2671
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Attorney Docket Number	8196-16

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